

AXI DDR3 Controller

The AXI DDR3 Controller provides access to DDR3 memory. It accepts the Read / Write commands from AXI and converts it into DDR3 access. While doing this it combines AXI burst transactions into single DDR access where ever possible to achieve the best possible performance from DDR3 memory subsystem.

DESCRIPTION

The AXI DDR3 Controller allows access of DDR3 memory through AXI Bus interface. The controller works as an intelligent bridge between the AXI host and DDR3 memory. It takes care of the DDR initialization and various timing requirements of the DDR3 memory. The controller implements multiple schemes to increase the effective memory throughput. These schemes include combining and reordering the Read/Write commands. It operates all the memory banks in parallel for attaining the maximum throughput from the memory and minimizes the effect of precharge/refresh and other DDR internal operations.

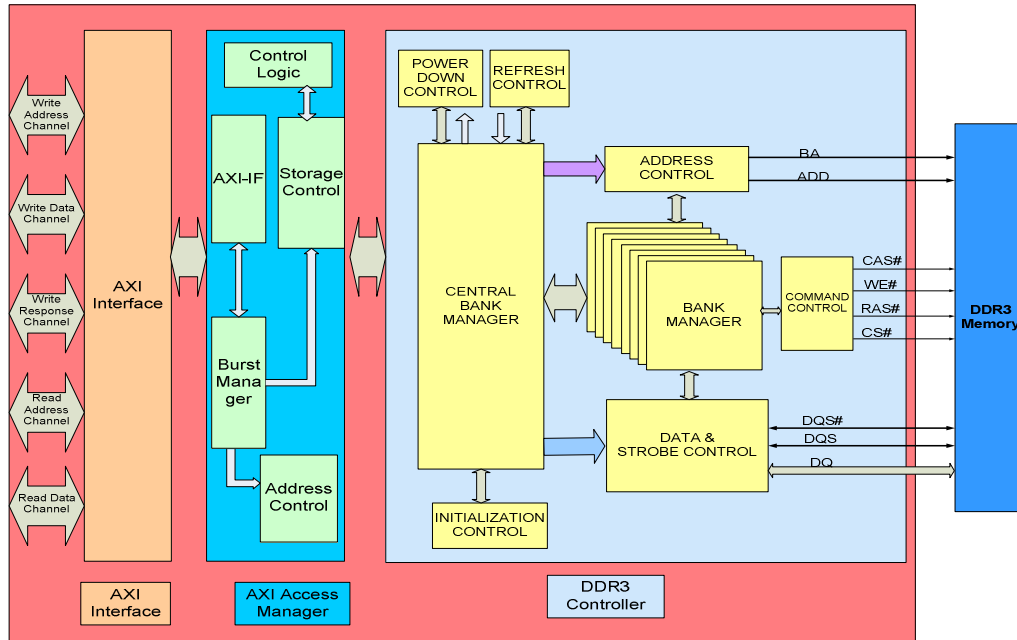
TECHINCAL DETAILS

- Gate Count
 - ASIC TSMC 90 nm Gate Count 34K
- Clock support
 - AXI clock 133 MHz to 400 MHz
 - DDR3 Data Rate of 800 Mbits/Sec supported

KEY FEATURES

- High memory throughput achieved via Parallel operation of all the banks and reordering of commands in the controller to ensure the maximum utilization of the DDR Memory
- Pipelined operation across the complete design to ensure the highest performance
- **DDR Interface**
 - Supports all standard DDR3 (x4,x8,x16) SDRAMs
 - Supports power down modes
 - Run-time configurable timing parameters and memory settings
 - Automatic generation of initialization and refresh sequences
 - All burst lengths (4 & 8) supported
- **AXI Interface**
 - Supports AMBA 3 AXI protocol 32 bit Data Width
 - Does re-mapping/combines the AXI Burst transactions into memory transactions by understanding the memory architecture
 - Supports unaligned transactions
 - Supports multiple outstanding transactions
 - Supports delayed Writes(Independent AXI command and Data Channel)

BLOCK DIAGRAM



DELIVERABLES

Verilog RTL/Synchronous Design

Test Plan, Test Bench, Test Cases & Test Results

Architecture Doc & LLD of Individual Blocks

ISE & DC Synthesis Scripts

APPLICATIONS

- **Mobile:** The portable and handheld markets require innovative, low cost solutions on a tight power budget.
- **Consumer:** Digital entertainment and multi-media markets call for fast access to memory enabling flexibility and fast time-to-market
- **Enterprise:** Communications, Storage, and high-end computing markets require high performance memory (DDR) solutions
- **Data Processing :** One of the most significant factors in the success of today's system-on-chip (SoC) designs is the ability to deliver efficient access to off-chip DDR memories
- **Security & Surveillance:** Security & Surveillance devices need considerable amount of fast storage for further processing

CONTACT DETAILS
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