

SATA Host Controller

Serial ATA (Serial Advanced Technology Attachment) is a computer bus technology primarily designed for transfer of data to and from Hard Disk Drives (HDD). Serial ATA host controllers and devices communicate over high-speed serial Link, up to 3Gbps. The “SATA Host controller” IP from HCL, handles the data movement between system memory and SATA device.

DESCRIPTION

“SATA Host controller” IP implements transport layer and link layer functions as defined in SATA specification revision 2.6. The IP has AMBA AHB interface on the application side and SAPIs/vendor specific PHY interface on the Physical layer side. The IP is compliant to SATA-AHCI 1.1 specification. The AHCI is a native SATA register-interface that simplifies the host controller design and provides a clean interface between hardware and software.

TECHNICAL DETAILS

ASIC

Gate Count (TSMC 0.13 μ) → 48K Gates

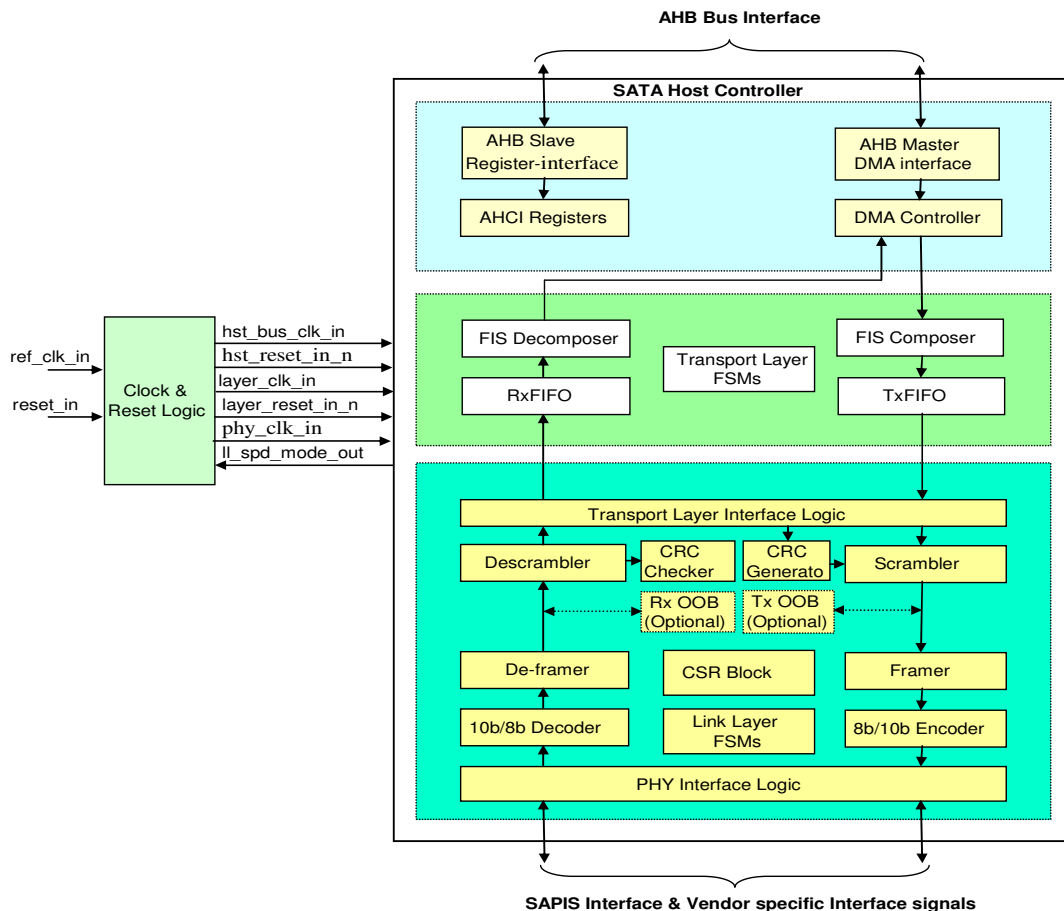
FPGA

LUT Count (Virtex-5) → 5931

KEY FEATURES

- Implements both Link layer and Transport layer of SATA specification revision 2.6
- Fully compliant to SATA (Gen1) 1.5Gbps and (Gen2) 3Gbps standards
- Supports Native Command Queuing (FPMMA)
- Supports ATAPI commands
- Supports power management functions (Partial and Slumber)
- Supports the DMA and PIO commands
- Supports speed negotiation
- Supports Far-end Retimed loopback
- Supports both Near-end & Far-end analog front-end loopback
- 256 deep FIFOs (Transmit, Receive) on the Transport layer (configurable)
- Descriptor based DMA engine that is compliant to AHCI register set
- Supports SAPIs interface at the PHY side (configurable)
- Provision to support vendor specific PHY interface signals
- PHY interface data width of Link layer is configurable to 10 / 20 / 40 bits.
- Supports AMBA AHB master/slave interface at the application side (AHB Master for DMA & AHB Slave for control & status registers)
- Fully compliant to AHCI specification (version 1.1), supports One port
- Supports 32 outstanding commands
- 8b/10b coding on the Link layer (option to disable the 8b/10b coding)
- CONTp and data scrambling to reduce EMI
- Both the Link and Transport layer supports Error reporting and Error recovery
- Supports configurable timer for power management
- Supports Interrupt to Host processor

BLOCK DIAGRAM



DELIVERABLES

HDL files (Source code) – Optional (based on the pricing model).
Synthesized Netlist
Synthesis scripts (Optional)
Complete Verification Environment – Verilog PLI based
Coverage Reports, Test Reports
IP User Manual

APPLICATIONS

- **Storage:** High capacity SATA based storage to make a cost effective storage solution for business applications.
- **Consumer:** Digital entertainment and multi-media markets like Set Top Box, Digital Video Recorders for fast access to external memory.

CONTACT DETAILS
ashok.madaan@hcl.in