

I2C -2.1 Controller

The I2C Controller provides access to devices with I2C interface. It accepts the Read / Write commands from APB and converts it to the serial I2C access. The controller supports High speed mode with maximum 3.4 Mbps throughput and it is down compatible with fast mode (400kbps) and standard mode (100kbps).

DESCRIPTION

The synchronous 2 bit I2C bus is a serial bus which supports the bit transfer rate up to 3.4Mbps. The I2C controller interfaces to the host through AMBA-APB bus. The host programs all the control and configuration register using APB bus. Depending on the data transfer direction the controller initiates the transaction. The controller is responsible for converting the 8 bit data from host to serial data or serial data from I2C bus to 8 bit data for the host.

The APB – I2C is a master/slave interface that enables synchronous serial communication with the other master or slave I2C peripherals having I2C compatible interface. Device states are read by the APB using status registers that reflect the completion of I2C transfers. Controller also supports the interrupt pin for indicating the transaction completion or any error in the controller.

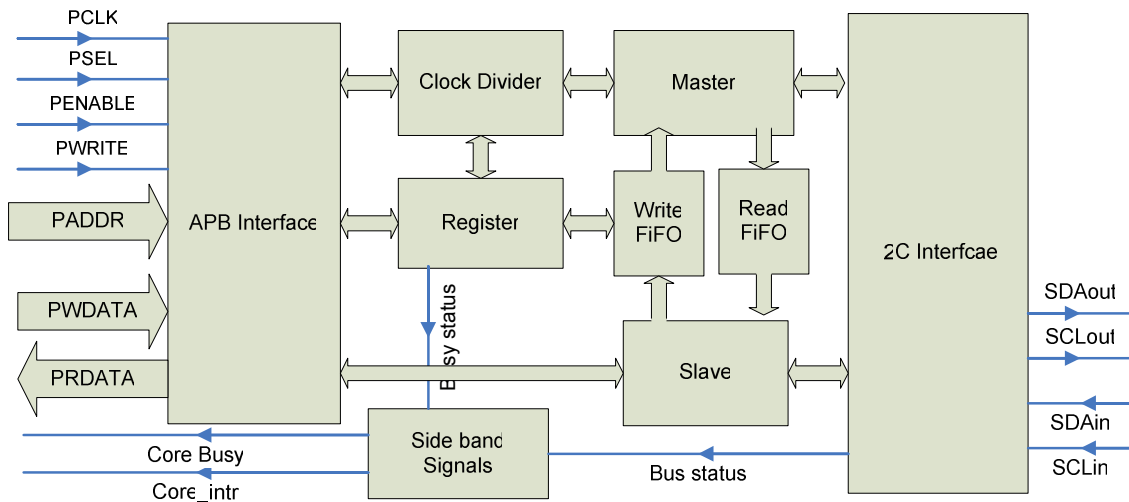
TECHINCAL DETAILS

ASIC
FPGA
Gate Count (Virtex-4)

KEY FEATURES

- **I2C Interface**
 - Compliant with I2C specification version 2.1
 - Supports a simple bi-directional 2-wire bus for efficient inter-IC control
 - Supports a Clock generation circuitry to drive I2C clock from APB clock
 - Supports 100kbps bit transfer rate in the standard mode, 400kbps in the fast mode and 3.4Mbps in the High speed mode.
- **APB Interface**
 - nx8 FIFO to accelerate the data transfer from and to I2C and APB with programmable FIFO watermark.
 - Compliant with AMBA-APB (ver-2.0) for integration with SOC implementations
 - Supports APB bus speed up to 100 MHz
 - Device States are read by periodic polling mechanism or using the interrupt pin.

BLOCK DIAGRAM



DELIVERABLES

I2C-2.1 compliant RTL source code in Verilog for following:

- Master and Slave combined core
- Master only core
- Slave only core

Synopsys DC synthesis scripts

Verification Environment with following components:

- Testbench
- APB BFM
- I2C slave Application
- I2C Bus analyser
- Test cases, regression scripts

- User manuals
- Design Docs

APPLICATIONS

- This I2C controller can be integrated with a SOC for consumer, networking or security application.

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